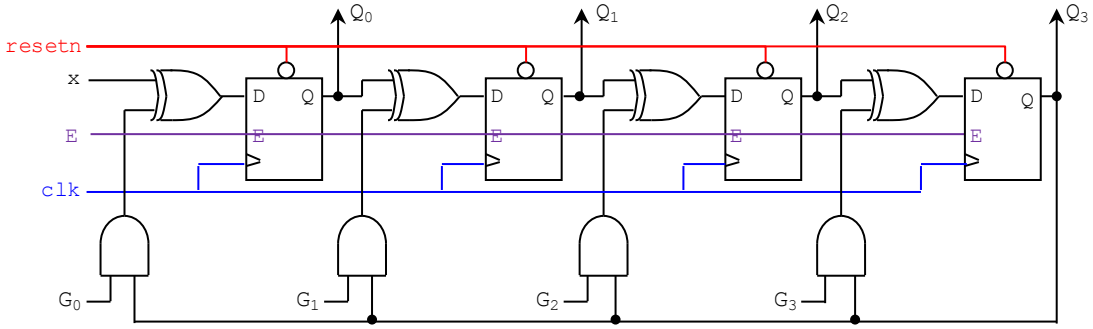
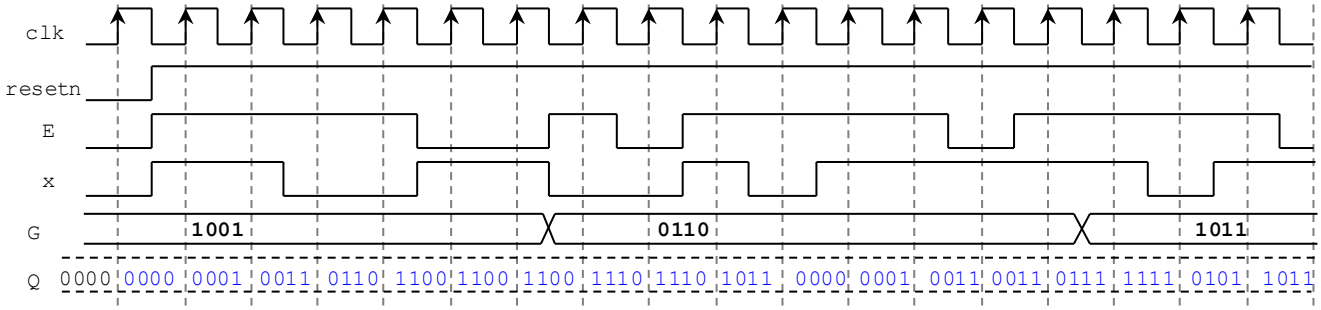
Solutions - Homework 4

(Due date: November 21st (001), November 20th (006) @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (14 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0$, $Q = Q_3Q_2Q_1Q_0$.



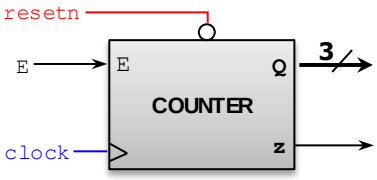


PROBLEM 2 (18 PTS)

Design a counter using a Finite State Machine (FSM):

Counter features:

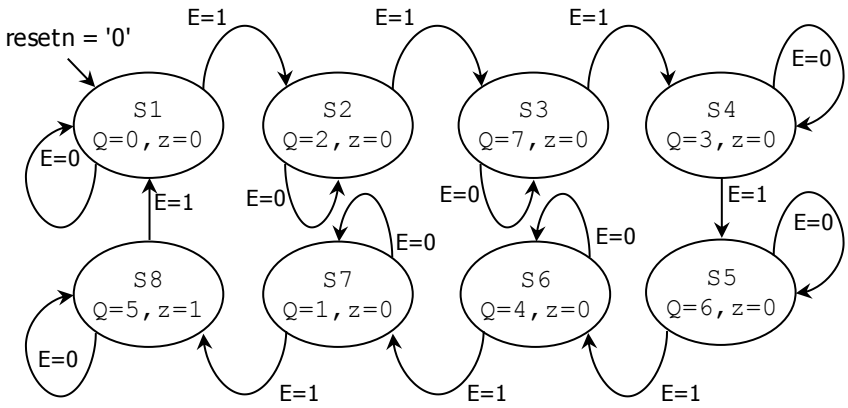
- ✓ Count: **000**, 010, 111, 011, 110, 100, 001, 101, **000**, 010, 111, …
- ✓ $resetn$: Asynchronous active-low input signal. It initializes the count to "000"
- ✓ Input E: Synchronous input that increases the count when it is set to '1'.
- ✓ output z: It becomes '1' when the count is 101.



- Provide the State Diagram (any representation), State Table, and the Excitation Table. Is this a Mealy or a Moore machine? Why? (10 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

- *State Diagram, State Table, State Assignment, and Excitation Table*:

S1: Q = 000
S2: Q = 001
S3: Q = 010
S4: Q = 011
S5: Q = 100
S6: Q = 101
S7: Q = 110
S8: Q = 111



The output z only depends on the present State. Thus, it is a Moore FSM.

E	PRESENT STATE	NEXT STATE	z
0	S1	S1	0
0	S2	S2	0
0	S3	S3	0
0	S4	S4	0
0	S5	S5	0
0	S6	S6	0
0	S7	S7	0
0	S8	S8	1
1	S1	S2	0
1	S2	S3	0
1	S3	S4	0
1	S4	S5	0
1	S5	S6	0
1	S6	S7	0
1	S7	S8	0
1	S8	S1	1

E	PRESENT STATE $Q_2Q_1Q_0(t)$	NEXTSTATE $Q_2Q_1Q_0(t+1)$	z
0	0 0 0	0 0 0	0
0	0 0 1	0 1 0	0
0	1 1 1	1 1 1	0
0	0 1 1	0 1 1	0
0	1 1 0	1 1 0	0
0	1 0 0	1 0 0	0
0	0 0 1	0 0 1	0
0	1 0 1	1 0 1	1
1	0 0 0	0 1 0	0
1	0 1 0	1 1 1	0
1	1 1 1	0 1 1	0
1	0 1 1	1 1 0	0
1	1 1 0	1 0 0	0
1	1 0 0	0 0 1	0
1	1 0 1	1 0 1	0
1	0 0 1	0 0 0	1

- *Excitation equations, minimization, and circuit implementation*:

$Q_2(t+1) \leftarrow \bar{E}Q_2 + E\overline{Q_2}Q_0 + EQ_1\overline{Q_0}$
$Q_1(t+1) \leftarrow Q_1Q_0 + \bar{E}Q_1 + E\overline{Q_2}\,\overline{Q_0}$
$Q_0(t+1) \leftarrow \bar{E}Q_0 + Q_0\overline{(Q_1 \oplus Q_2)} + E\overline{Q_0}(Q_1 \oplus Q_2)$
$z = Q_2\overline{Q_1}Q_0$

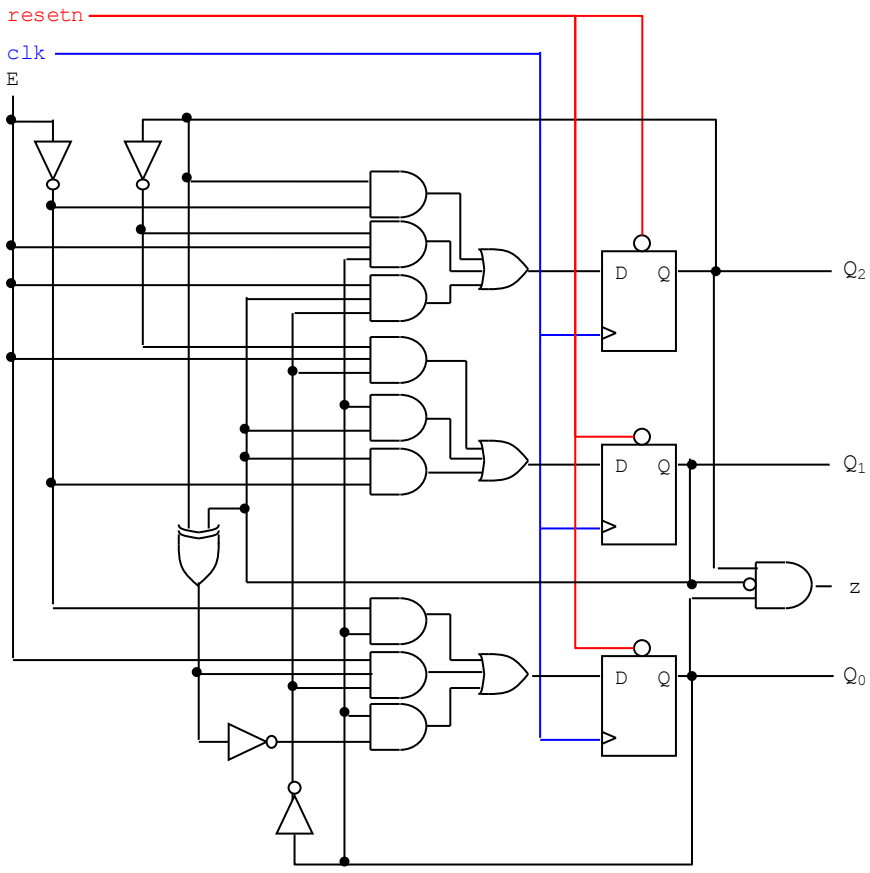
$Q_2(t+1)$

Q_1Q_0 \ EQ$_2$	00	01	11	10
00	0	1	0	0
01	0	1	0	1
11	0	1	0	1
10	0	1	1	1

$Q_1(t+1)$

Q_1Q_0 \ EQ$_2$	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	1	1	1
10	1	1	0	1

- *Circuit Implementation*:



$Q_0(t+1)$

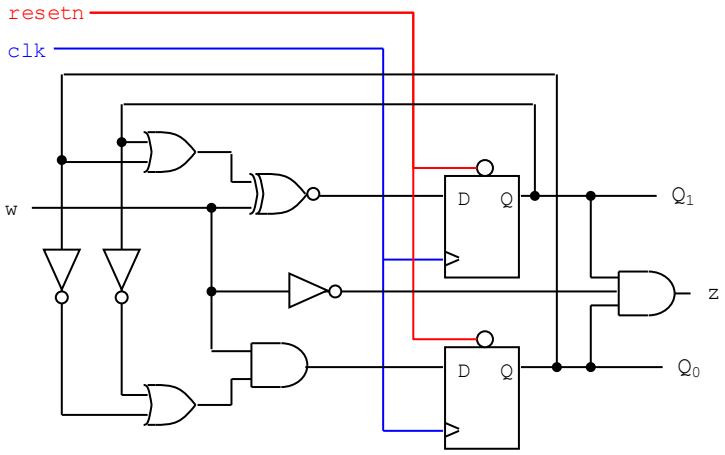
Q_1Q_0 \ EQ$_2$	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	1	1	1	0
10	0	0	0	1

z

Q_1Q_0 \ EQ$_2$	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	0	0	0	0
10	0	0	0	0

PROBLEM 3 (20 PTS)

- Given the following State Machine Diagram. (10 pts).
  - ✓ Provide the State Diagram (any representation) and the Excitation Table,
  - ✓ Provide the Excitation equations and the Boolean equation for z.



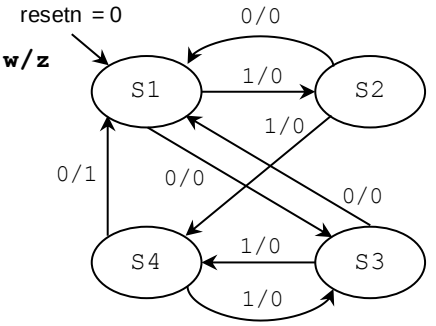
w: input, z: output, Q_1Q_0: state.

$Q_1(t+1) \leftarrow \overline{(Q_1 + Q_0) \oplus w}$
$Q_0(t+1) \leftarrow \overline{Q_1 Q_0} w$
$z = \bar{w} Q_1 Q_0$

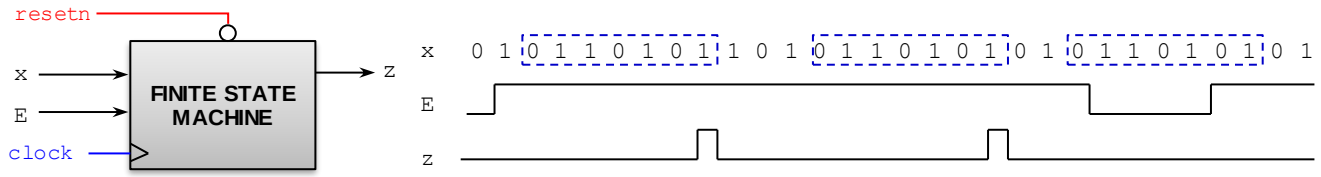
State Assignment:
S1: Q=00 S2: Q=01
S3: Q=10 S4: Q=11

PRESENT STATE w Q_1Q_0 (t)	NEXTSTATE Q_1Q_0 (t+1)	z
0 0 0	1 0	0
0 0 1	0 0	0
0 1 0	0 0	0
0 1 1	0 0	1
1 0 0	0 1	0
1 0 1	1 1	0
1 1 0	1 1	0
1 1 1	1 0	0

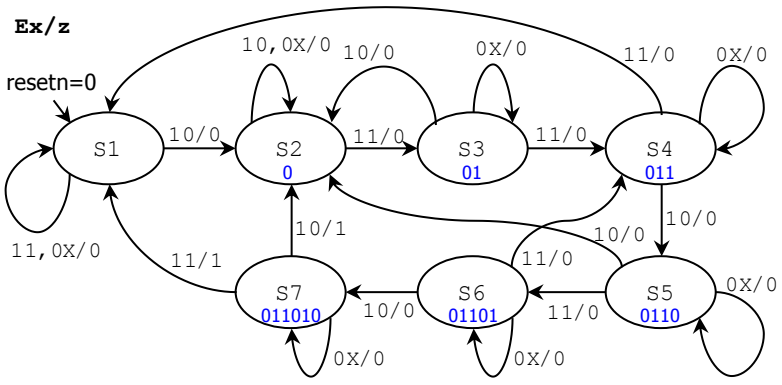
w	PRESENT STATE	NEXT STATE	z
0	S1	S3	0
0	S2	S1	0
0	S3	S1	0
0	S4	S1	1
1	S1	S2	0
1	S2	S4	0
1	S3	S4	0
1	S4	S3	0



- **Sequence detector**: Provide the State Diagram (any representation) and the Excitation Table of a circuit with inputs x and E and output z. The machine has to generate $z = 1$ when it detects the sequence 0110101. Right after the sequence is detected, the circuit looks for a new sequence. (10 pts).
  The signal E is an input enable: It validates the input x, i.e., if $E = 1$, x is valid, otherwise x is not valid.



S1: Q = 000
S2: Q = 001
S3: Q = 010
S4: Q = 011
S5: Q = 100
S6: Q = 101
S7: Q = 110



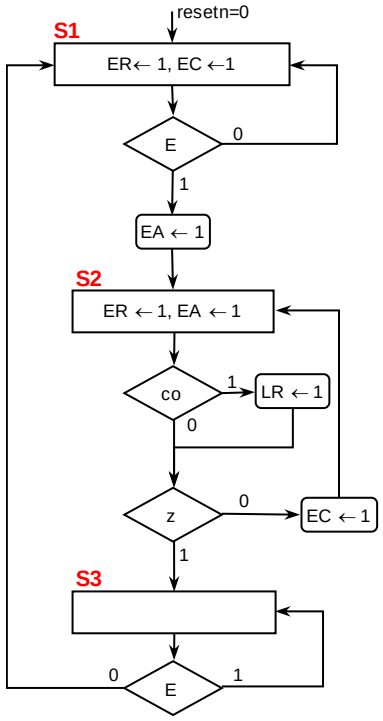
E	x	PRESENT STATE	NEXT STATE	z
0	X	S1	S1	0
0	X	S2	S2	0
0	X	S3	S3	0
0	X	S4	S4	0
0	X	S5	S5	0
0	X	S6	S6	0
0	X	S7	S7	0
1	0	S1	S2	0
1	0	S2	S2	0
1	0	S3	S2	0
1	0	S4	S5	0
1	0	S5	S2	0
1	0	S6	S7	0
1	0	S7	S2	0
1	1	S1	S1	0
1	1	S2	S3	0
1	1	S3	S4	0
1	1	S4	S1	0
1	1	S5	S6	0
1	1	S6	S4	0
1	1	S7	S1	1

E x $Q_2Q_1Q_0$(t)	$Q_2Q_1Q_0$(t+1) z
0 X 0 0 0	0 0 0 0
0 X 0 0 1	0 0 1 0
0 X 0 1 0	0 1 0 0
0 X 0 1 1	0 1 1 0
0 X 1 0 0	1 0 0 0
0 X 1 0 1	1 0 1 0
0 X 1 1 0	1 1 0 0
1 0 0 0 0	0 0 1 0
1 0 0 0 1	0 0 1 0
1 0 0 1 0	0 0 1 0
1 0 0 1 1	1 0 0 0
1 0 1 0 0	0 0 1 0
1 0 1 0 1	1 1 0 0
1 0 1 1 0	0 0 1 0
0 1 0 0 0	0 0 0 0
0 1 0 0 1	0 1 0 0
0 1 0 1 0	0 1 1 0
0 1 0 1 1	0 0 0 0
0 1 1 0 0	1 0 1 0
0 1 1 0 1	0 1 1 0
0 1 1 1 0	0 0 0 1
X X 1 1 1	X X X X

PROBLEM 4 (15 PTS)

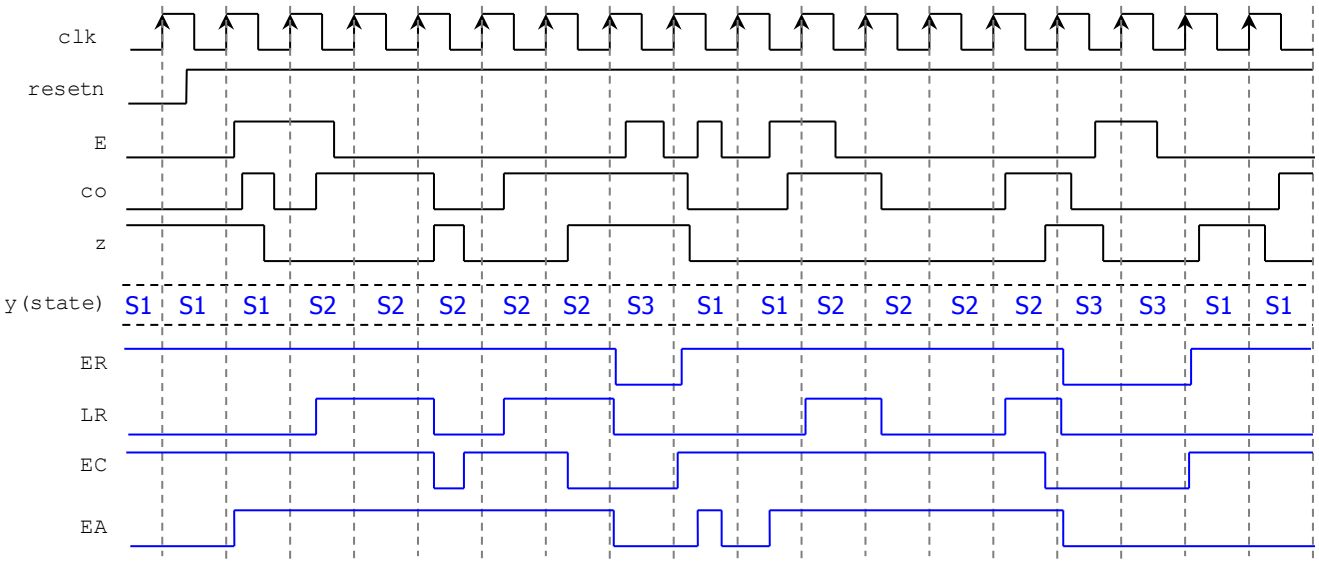
- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
   port ( clk, resetn: in std_logic;
          z, E, co: in std_logic;
          ER,LR,EC,EA: out std_logic);
end myfsm;
```



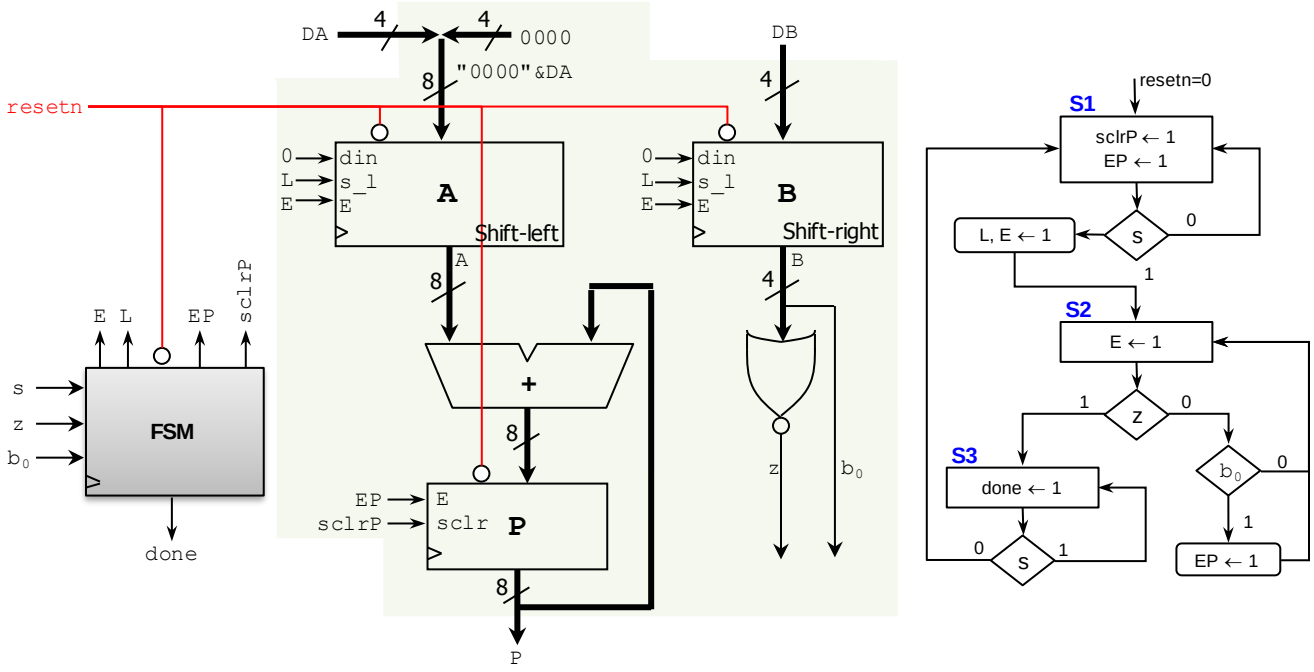

```
architecture behavioral of myfsm is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, z, E, co)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if E = '1' then y <= S2; else y <= S1; end if;

          when S2 =>
            if z = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if E = '1' then y <= S3; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, z, E, co)
  begin
      ER <= '0'; LR <= '0'; EC <= '0'; EA <= '0';
      case y is
         when S1 => ER <= '1'; EC <= '1';
                    if E = '1' then EA <= '1'; end if;

         when S2 => ER <= '1'; EA <= '1';
                    if co = '1' then LR <= '1'; end if;
                    if z = '0' then EC <= '1'; end if;

         when S3 =>
      end case;
  end process;
end behavioral;
```

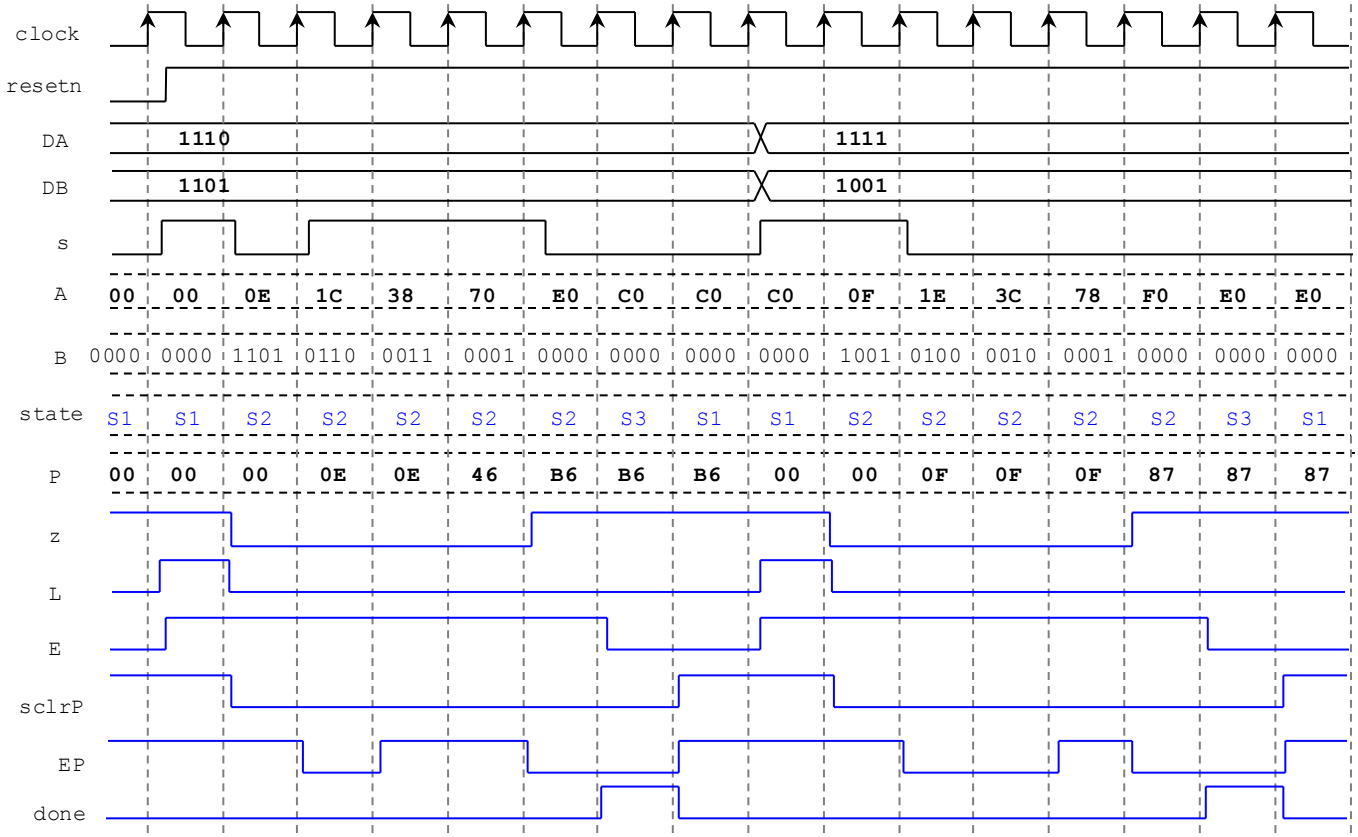
This is a Mealy FSM. The outputs LR, EC, EA depend on the input as well as on the present state.



PROBLEM 5 (18 PTS)

- Complete the following timing diagram (`A` and `P` are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
  Register (for `P`): $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.
  Parallel access shift registers (for `A` and `B`): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift





PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than two pages, single-spaced, 2 columns). This report should contain the current status of the project. You **MUST** use the provided template (`Final Project – Report Template.docx`).